SKYWORKS

DATA SHEET

AAT2491

Dual N-Channel HV Cascode-Clamp, Lateral TrenchDMOS Array

General Description

The AAT2491 is a monolithically integrated dual N-channel high-voltage cascode-clamp lateral TrenchDMOS array. The dual-channel AAT2491 monolithically integrates both current-sink (CS) and high-voltage cascode-clamp (CC) power MOSFETs required for reliably driving a large series string of LEDs as used in a variety of lighting and display backlight applications.

The AAT2491's low-voltage current-sink (CS) device, required for closed-loop current control in large panel LED driver applications, is constructed using Skyworks' robust lateral TrenchDMOS process featuring superior hot carrier performance needed for reliable constant-current operation. It has a low on resistance, typically 1.5Ω, facilitating constant current operation over a wide dynamic range. The low-voltage current-sink Lateral TrenchDMOS process features a low threshold voltage ($V_{GS(ON)}$) and can be driven directly from a 5V supply.

The high-voltage cascode-clamp TrenchDMOS device has a drain-to-source voltage rating of 150V. With a 12V gate drive, it exhibits a typical on-resistance of 5Ω.

In high-voltage LED backlighting applications for TVs and large-screen LCD panels, the AAT2491 TrenchDMOS array allows control of two series strings of LEDs with up to 40 LEDs per string. Each series connected TrenchDMOS pair comprises a current sink device with its gate actively driven by a backlight driver IC (such as the AAT2430A-1 or the AAT2405).

To facilitate direct temperature measurement of the AAT2491 in a system, a series connected string of P-N junction diodes is included with both anode and cathode connections available separate from the supply.

The AAT2491 is available in a Pb-free, 16-pin SOP-EP package with 1.27mm pin pitch.

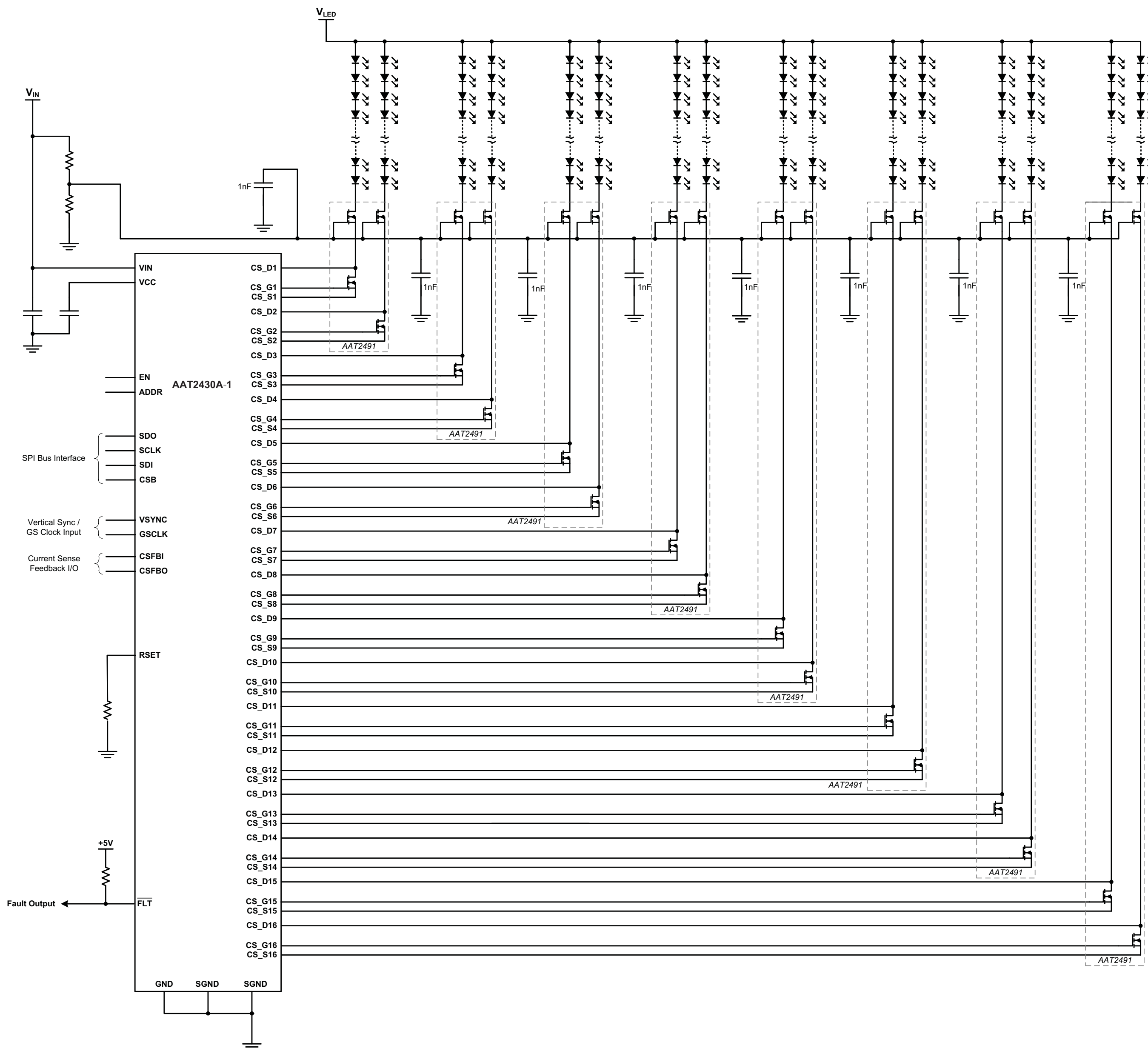
Features

- Low-Voltage Current Sink TrenchDMOS
  - Low $R_{DS(ON)}$ for Low Dropout Operation
    - 1.5Ω @ V_{GS} = 5V (typical)
- High-Voltage Cascode-Clamp TrenchDMOS
  - $BV_{DSS(MAX)}$ = 150V
  - Low $R_{DS(ON)}$
    - 5Ω @ V_{GS} = 12V (typical)
- Up to 240mA per channel at TA = 25°C
- 16-pin SOP-EP, 1.27mm Pitch Package
- -40°C to +85°C Temperature Range

Applications

- LCD TV Panels
- LCD Monitors
- White LED Backlighting
- High-Voltage LED Lighting

Typical Application Circuit[1]



1. Simplified for clarity.

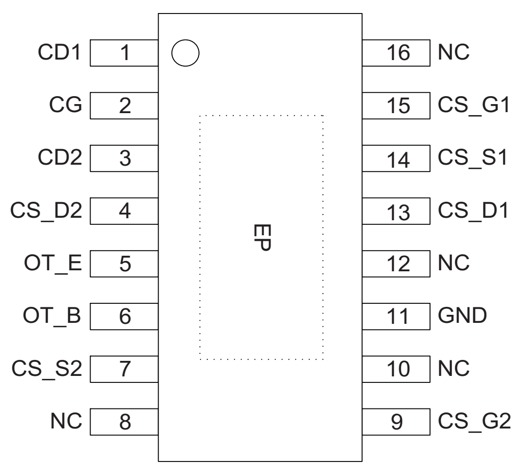
Dual N-Channel HV Cascode-Clamp, Lateral TrenchDMOS Array

Pin Descriptions

Pin #	Symbol	Function	Description
1	CD1	I	Voltage clamp MOSFET 1 drain.
2	CG	I	Voltage clamp MOSFET common gate drive. Bypass with 1nF ceramic capacitor to ground.
3	CD2	I	Voltage clamp MOSFET 2 drain.
4	CS_D2	O	Current sink MOSFET 2 sense.
5	OT_E	I/O	Cathode connection to temperature PN diode.
6	OT_B	I/O	Anode connection to temperature PN diode.
7	CS_S2	O	Current sink MOSFET 2 controlled current sink.
8, 10, 12, 16	NC		Not connected.
9	CS_G2	I	Current sink MOSFET 2 gate drive.
11	GND	GND	General ground pin.
13	CS_D1	O	Current sink MOSFET 1 sense.
14	CS_S1	O	Current sink MOSFET 1 controlled current sink.
15	CS_G1	I	Current sink MOSFET 1 gate drive.
EP	EP	GND	Exposed paddle. Connect to PCB GND plane.

Pin Configuration

SOP-EP-16
(Top View)



Absolute Maximum Ratings[1]

T_A = 25°C unless otherwise noted.

Symbol	Description	Value	Units
High Voltage Cascode MOSFET			
V_{CD1}, V_{CD2}	Voltage Clamp MOSFET Drain Voltage	150 to -0.3	V
V_{CG}	Voltage Clamp MOSFET Common Gate Driver Voltage	15 to -0.3	
Low Voltage Current Sink MOSFET			
V_{GS}	Gate-Source Voltage	15 to -0.3	V
Both			
I_D	Continuous current @ T_J = 150°C[2,3], two channels in parallel[4]	480	mA
θ_{JA}	Thermal Resistance[5,6]	52.0	°C/W
P_D	Maximum Power Dissipation[5,6]	2.4	W
T_J	Maximum Junction Operating Temperature	-40 to +150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec.)	300	
Temperature Sense Diode String			
V_f	Diode Reverse Bias Voltage	5.5 to -0.3	V

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied.
2. Based on long-term current density limitation.
3. Both MOSFETS in parallel.
4. The test condition is V_{CG}=V_{CS_Gx}=12V, V_{CD1}=V_{CD2}=5V, in the case when the V_{CDx} voltage is differ from 5V, the I_D(max) value can be obtained from V_{CDx} x I_D(max) =2.4W at T_A=25°C
5. The thermal data is extracted from a 2-layer FR4 board.
6. The thermal resistance measured in accordance with EIA/JESD 51 series.

Electrical Characteristics

T_J = 25°C unless otherwise noted.

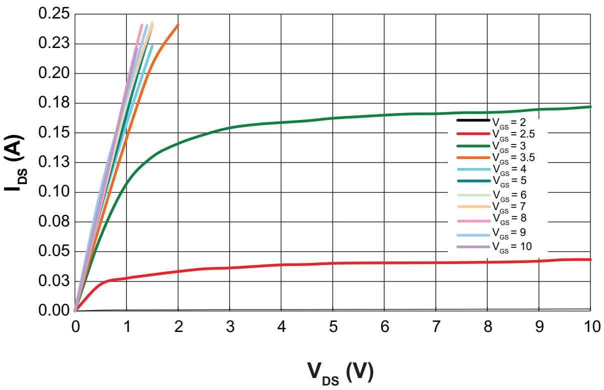
Symbol	Description	Conditions	Min	Typ	Max	Units
High Voltage Cascode MOSFET						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{CG} = 12V, V_{CS_G} = V_{CS_S} = 0V, I_{CD} = 10µA	150			V
V_{CG}	Operating CG Pin Voltage Range		5	12	13.2	
$R_{DS(ON)}$	Drain-Source ON Resistance[1]	V_{CG} = 10V, V_{CS_D} = 0V, I_{CD} = 150mA		5		Ω
$V_{GS(th)}$	Gate Threshold Voltage	V_{CG} = V_{CD}, V_{CS_D} = 0V, I_{CD} = 250µA	1.1	1.8		V
I_{GSS}	Gate Leakage Current	V_{CG} = 12V, V_{CD} = V_{CS_D} = 0V			100	nA
I_{DSS}	Drain-Source Leakage Current	V_{CD} = 100V, V_{CG} = V_{CS_D} = 0V			1	µA
g_{fs}	Forward Transconductance	V_{CD} = 25V, V_{CS_D} = 0V, I_{CD} = 150mA		0.3		S
Low Voltage Current Sink MOSFET						
V_{GS}	V_{CS_Gx} Recommended Operating Voltage Range				14	V
$R_{DS(ON)}$	Drain-Source ON Resistance[1]	V_{CS_G} = 5V, V_{CS_S} = 0V, I_{CS_D} = 150mA		1.5		Ω
$I_{D(ON)}$	On-State Drain Current[1]	V_{CS_G} = 5V, V_{CS_S} = 0V, V_{CS_D} = 5V	200			mA
$V_{GS(th)}$	Gate Threshold Voltage	V_{CS_G} = V_{CS_D}, V_{CS_S} = 0V, I_{CS_D} = 250µA		1.6		V
I_{GSS}	Gate Leakage Current	V_{CS_G} = 12V, V_{CS_D} = V_{CS_S} = 0V			100	nA
I_{DSS}	Drain-Source Leakage Current	V_{CG} =12V, V_{CD} =100V V_{CS_G} = V_{CS_S} = 0V			1	µA
g_{fs}	Forward Transconductance	V_{CS_D} = 5V, V_{CS_S} = 0V, I_{CS_D} = 150mA		0.45		S
Temperature Sense Diode String						
V_f	Forward Bias Voltage	I = 300µA		3.08		V
ΔV_f	Delta Forward Bias Voltage (V_F @150°C - V_F @25°C)	I = 300µA		680		mV

1. Pulse test: Pulse width = 300µs.

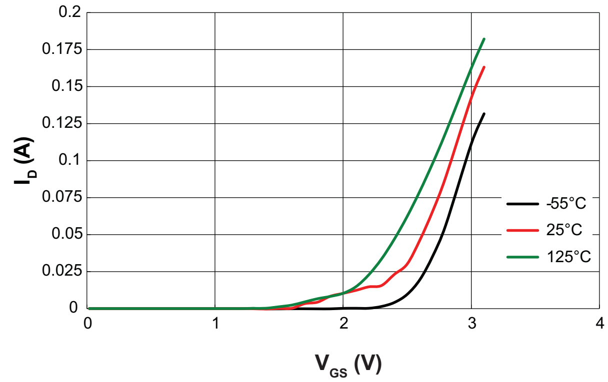
Dual N-Channel HV Cascode-Clamp, Lateral TrenchDMOS Array

Typical Characteristics (High Voltage Cascode MOSFET)

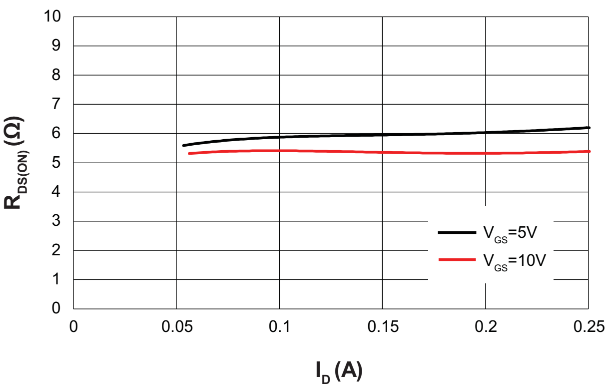
Output Characteristics



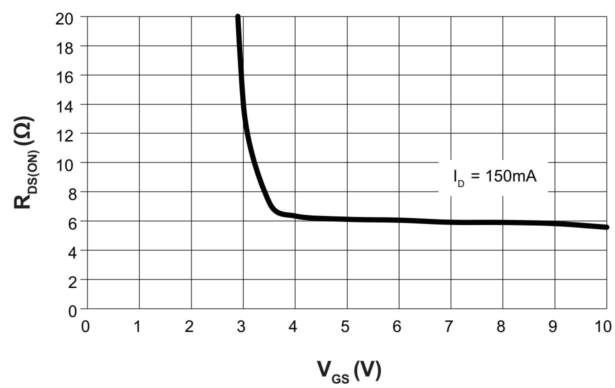
Transfer Characteristics



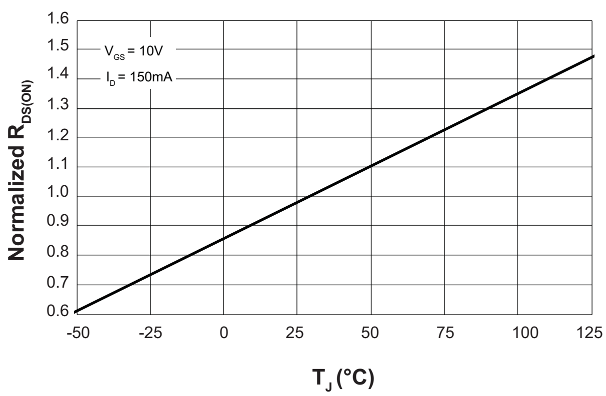
On-Resistance vs Drain Current



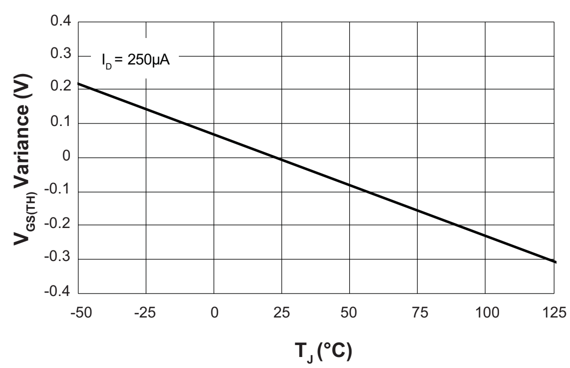
On-Resistance vs Gate-Source Voltage



On-Resistance vs Junction Temperature



Threshold Voltage vs Junction Temperature



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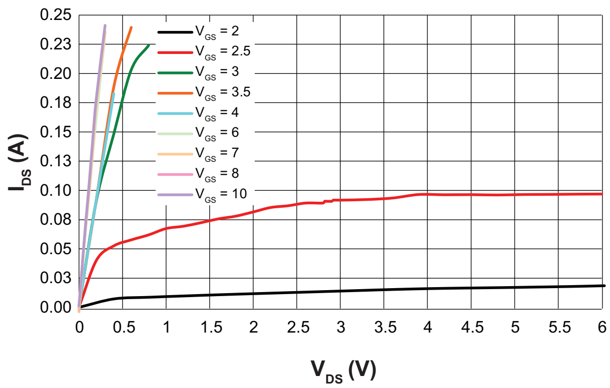
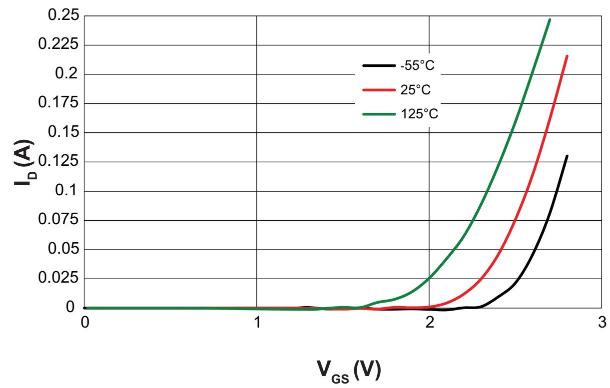
Dual N-Channel HV Cascode-Clamp, Lateral TrenchDMOS Array

Typical Characteristics (Low Voltage Cascode MOSFET)

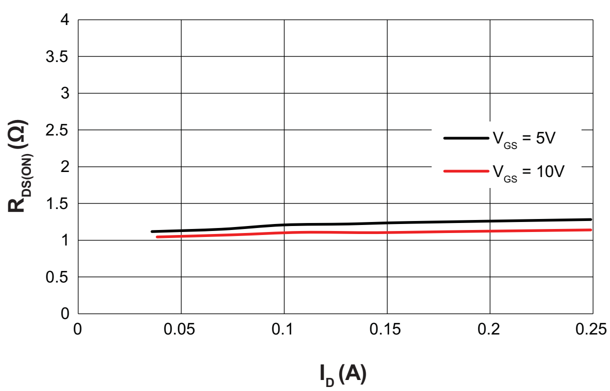
Output Characteristics



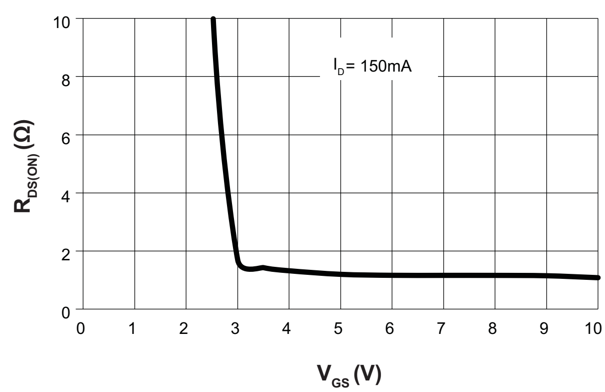
Transfer Characteristics



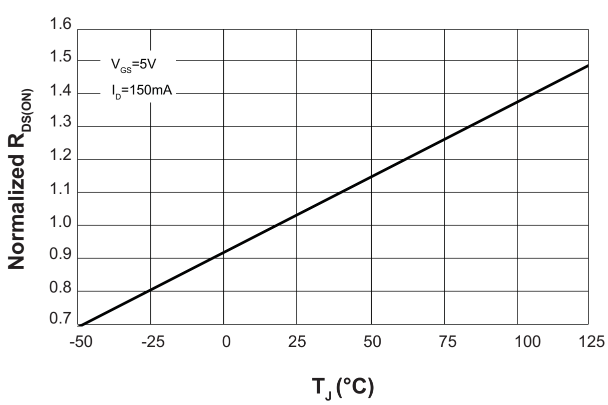
On-Resistance vs Drain Current



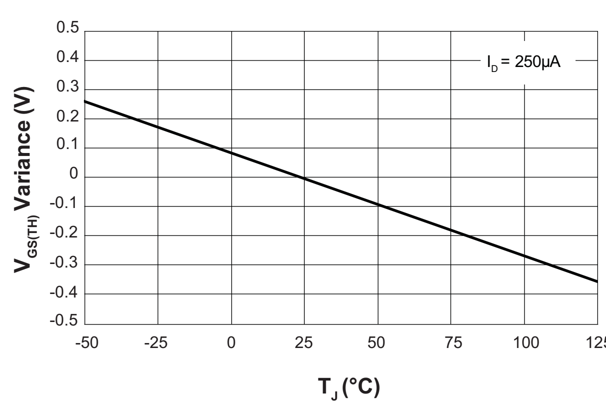
On-Resistance vs Gate-Source Voltage



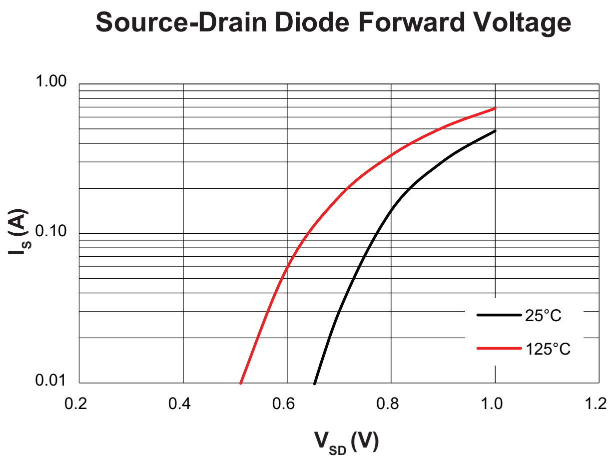
On-Resistance vs Junction Temperature



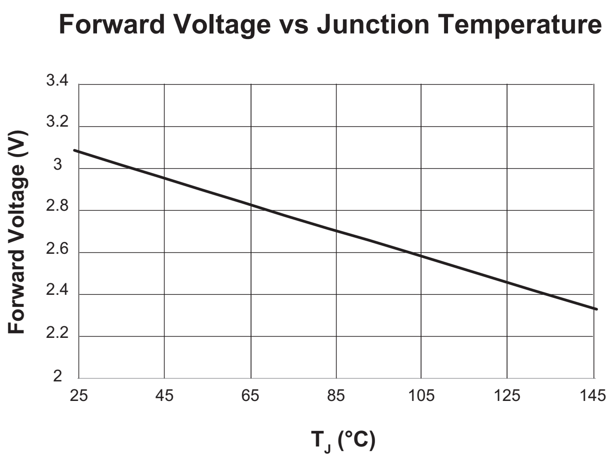
Threshold Voltage vs Junction Temperature



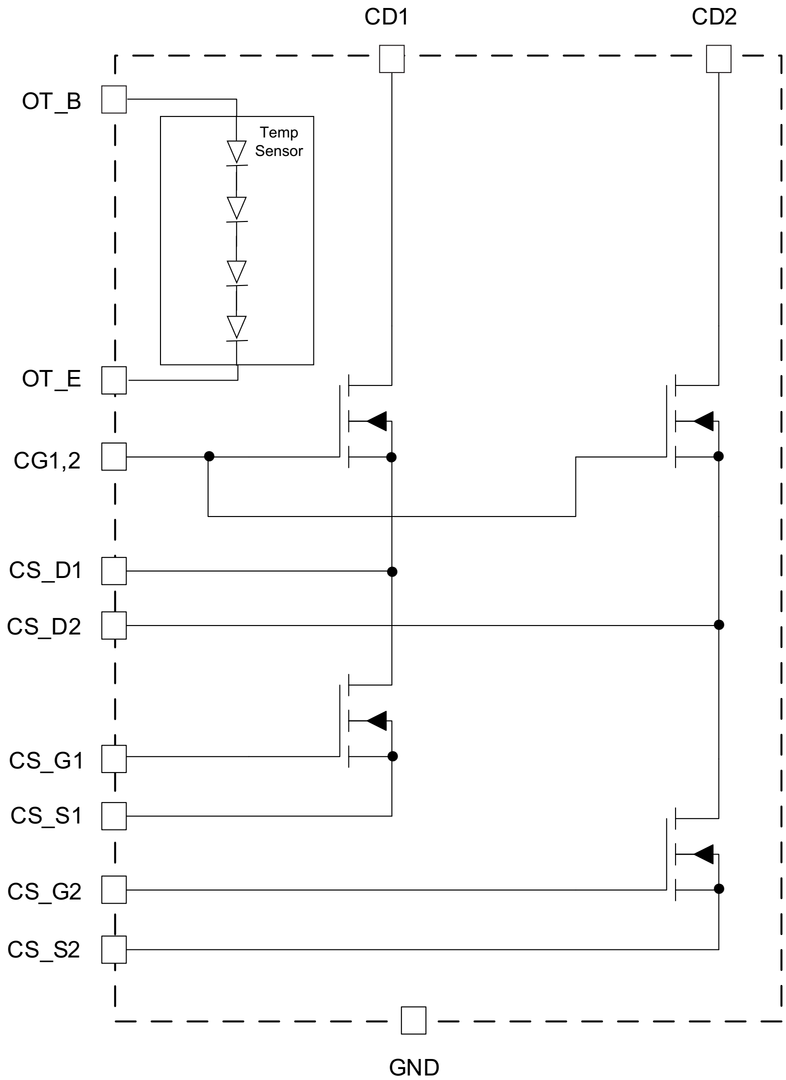
Typical Characteristics (Low Voltage Cascode MOSFET)



Typical Characteristics (Temperature Sense Diode String)



Functional Block Diagram



Functional Description

The AAT2491 is a dual cascode-clamp current sink MOSFET used to both protect and control the current in a series string of LEDs used in LCD backlighting applications. Replacing four discrete transistors, the AAT2491 comprises four lateral TrenchDMOS transistors in a popular SOP-EP-16 package with 1.27mm pin pitch.

The AAT2491 utilizes lateral TrenchDMOS transistors, which are avalanche-rugged, robust power devices, fabricated using Skyworks' patented ModularBCD process technology to integrate the transistor array. Lateral TrenchDMOS transistors exhibit hot carrier reliability superior to conventional surface MOSFET devices. All gate pins include ESD protection diodes but to avoid possible damage by a surge voltage on the high voltage cascode-clamp MOSFET gate, it is recommended to put a 1kΩ, or greater, series resistor between the power supply and the gate pin. (In case of using resistor divider to supply the voltage for the gate bias, the upper resistance will work as a series resistance.) The CG pin is also required to have a bypass capacitor (greater than or equal to 1nF) to the ground.

In high-voltage LED backlighting applications, the low side TrenchDMOS devices of the AAT2491 are normally used as part of a linear control and feedback circuit to regulate the current in each series string of LEDs according to the gate bias supplied by an LED driver integrated circuit (such as the AAT2430A-1 or the AAT2405). Since the source connections of the low side TrenchDMOS devices are separate from ground, the device is compatible with current sensing using either discrete sense resistors or I-Precise™ current monitoring and gate drive available in Skyworks' products, for improved accuracy.

The high-side cascode clamp TrenchDMOS devices are used to protect an LED driver IC from the high voltages present in HV LED backlighting systems. Such high voltages, generally ranging from 50V up to 150V, are needed for forward biasing LED strings having many series connected LEDs. During operation, most of this high voltage is dropped across the conducting LEDs and not across the silicon transistors driving the LEDs. When the LEDs are not conducting (or conducting low currents) or when one or more LEDs become shorted, a disproportionate amount of the voltage is impressed on the driver devices. Without the cascode-clamp, the current sink transistors may be permanently damaged.

Using cascode clamping, i.e. where a high voltage MOSFET is operated as a voltage follower, the maximum voltage impressed on any current sink device is safely limited. In such an application, each cascode clamp TrenchDMOS device has its gate biased to a fixed voltage $V_{G(CLAMP)}$ with its drain connected to the LED string and its source prewired in series with the current sink device. As the drain voltage rises in normal operation, the high-side transistor's source voltage V_S follows until the source voltage reaches a potential approximately one V_T (one threshold) below the fixed gate bias voltage, or $V_{G(CLAMP)} - V_T$. Above that potential, further drain voltage increases will not drive the source voltage any higher. For example if the gate is biased to 12V, the source can be driven to a potential no higher than 10V, thereby clamping the drain voltage of the low-side current sink to within safe operation range. It is required to put a 1nF bypass capacitor connected from CG pin to ground.

The AAT2491 includes a series string of four P-N junction diodes for monitoring die temperature. To facilitate simple, over-temperature monitoring, the diode string should be forward biased by a constant current or a resistor to approximately 300µA. The voltage of the conducting diode string can easily be monitored with a comparator to determine if an over-temperature condition has occurred, specifically where the diode voltage drops below a pre-specified value. A characterization curve comparing the diode string forward voltage to temperature is included for reference.

Dual N-Channel HV Cascode-Clamp, Lateral TrenchDMOS Array

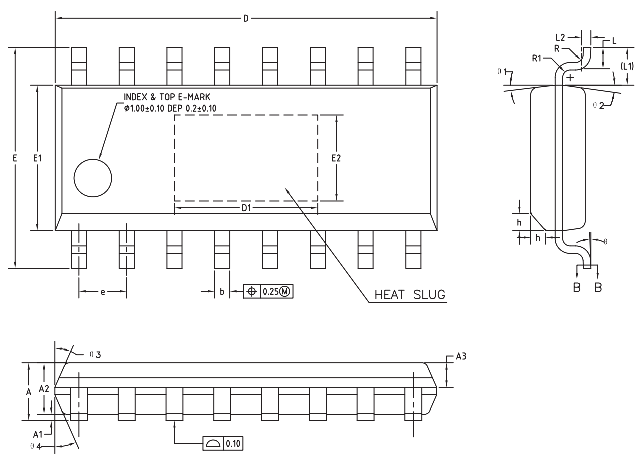
Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)[2]
SOP-EP-16	FAYW	AAT2491IAN-T1

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

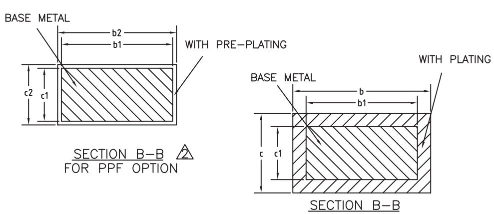
Package Information[3]

SOP-EP-16



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
2	A	1.35	1.52	1.70
2	A1	0.02	0.07	0.12
	A2	1.35	1.45	1.55
	A3	0.55	0.65	0.75
2	b	0.38	–	0.47
2	b1	0.37	0.40	0.43
2	b2	0.371	–	0.44
2	c	0.20	–	0.25
2	c1	0.19	0.20	0.21
2	c2	0.191	–	0.22
	D	9.86	9.96	10.06
	D1	3.30	3.81	4.00
	E	5.80	6.00	6.20
	E1	3.80	3.90	4.00
	E2	1.78	2.29	2.50
	e	1.27BSC		
	L	0.45	0.60	0.80
	L1	1.04REF		
	L2	0.25BSC		
	R	0.07	–	–
	R1	0.07	–	–
	h	0.30	0.40	0.50
	θ	0°	–	8°
	θ_1	6°	8°	10°
	θ_2	6°	8°	10°
	θ_3	5°	7°	9°
	θ_4	5°	7°	9°



NOTES:

2 1.ALL DIMENSIONS REFER TO JEDEC STANDARD MS–012 BC
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

2 2.'D1' AND 'E2' ARE VARIABLES DEPENDING ON DIE PAD SIZES.

All dimensions in millimeters.

1. FAYW = Fab, Assembly, Year and Week code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.